DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 30, 2009 has been entered.

Response to Arguments

2. Applicant's arguments filed October 30, 2009 have been fully considered but they are not persuasive.

3. Applicant argues that Levy (US 20040088469A1) fails to teach "wherein said switch is configured to distribute lanes dynamically during operation including data transmission" (p. 10).

In reply, the Examiner respectfully points out that the Examiner was unable to find any description of the switch distributing lanes dynamically during data transmission anywhere in the instant specification. The instant specification describes that the switch distributes lanes dynamically (p. 27, cited by Applicant on p. 11 of remarks), however, it does not describe that this is done during data transmission. Applicant states that support for these amendments are provided in at least the Figures and related text of the specification (p. 9), however, Applicant did not specifically point out which Figures and related text support these amendments, and the portion that Applicant did specifically point out on p. 11 of the remarks does not support the amendment, as discussed above. The Examiner requests for Applicant to specifically point out the portions of the specification that describe the amended limitation.

4. Applicant argues that Levy does not disclose the devices can be operating, -- i.e., processing or outputting data -- while the switch dynamically distributes the lanes in response to changes in bandwidth needs (p. 10).

In reply, the Examiner points out that Levy teaches that devices may initiate their port identification methods in response to events other than in response to power on reset, such as, for example, root reset or request to re-identify its ports [0042]. Therefore, devices do not have to turn off and then turn on in order to initiate their port identification methods. Therefore, devices can be powered on the entire time while they initiate their port identification methods. Since the devices are powered on the entire time, this is taken to mean that the devices are operating or processing the entire time. Levy teaches that a switch (116) is configured to distribute lanes, as discussed above. Levy teaches that the switch is configured to distribute different numbers of lanes to different ports of different devices, and can change this distribution [0075, 0042], and therefore the switch is configured to distribute lanes dynamically. Levy describes "port identification methods provide the system designer with fine grain control of bandwidth between devices" [0075], and therefore the lanes are distributed responsive to changes in bandwidth needs. Therefore, Levy teaches that the request to re-identify its ports is performed by a switch configured to distribute lanes dynamically during operation or processing to said plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by said video cards [0075, 0016, 0042].

5. Applicant argues that the alleged teaching from Levy do not necessarily flow port transmitters 116 performing port identification as required for inherency (p. 11).

In reply, the Examiner points out that Levy teaches that devices transmit data to other devices by connecting their port transmitters 116 to port receivers on other devices through links (Figs. 2-3) [0018, 0021]. Port identification is performed by a port receiving a child ID and updating the device mapping table to indicate which port on the device is connected to which port on which device as indicated by the child ID response received from the device that the device is to be connected to, and then connecting the ports as indicated by the mapping table in order to transmit data to the indicated device [0041, 0044, 0074, 0075]. Thus, in order to indicate which port of the device is connected to which port on which device for port identification, the ports need to determine where the port transmitters 116 are connected (Figs. 2-3) [0018, 0021]. Thus, ultimately, the port transmitters 116 are performing the port identification.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1, 41, and 48 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 recites "…wherein said switch is configured to distribute lanes dynamically during operation including data transmission…" Claims 41 and 48 also recite a similar limitation. The Examiner respectfully points out that the Examiner was unable to find

any description of the switch distributing lanes dynamically during data transmission anywhere in the instant specification. The instant specification describes that the switch distributes lanes dynamically, however, it does not describe that this is done during data transmission. The Examiner requests for Applicant to specifically point out the portions of the specification that describe this limitation.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1, 3-7, 29, 30, 32-34, 41, 44-48, and 50-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (US 20040088469A1), Stufflebeam (US006295566B1), and Grimaud (US005546530A).

11. As per Claim 1, Levy teaches chipset (104) for managing data transfers within computing device [0014]; scalable interconnect (Device 0) connecting to computing device [0021], scalable interconnect supporting a number of interconnect lanes [0021, 0018]; plurality of ports or high-

speed video card slots [0016] connected to interconnect [0021], high speed video card slots including at least one 1^{st} video card slot and 2^{nd} video card slot [0016]. According to Applicant's disclosure, "high speed video card slot" is defined as PCI Express video card slot [00057]. Levy teaches one or more devices (DEVICES 1-5) comprise video cards [0016]. Device interfaces of DEVICES 0-5 have ports that provide physical interface for establishing lanes between devices. Link comprises lanes which are grouped together to form communications path between devices [0018]. These links are PCI Express links [0001]. So, Levy teaches video cards are connected to system through PCI Express links, and so Levy is considered to teach PCI Express video card slots, which are high speed video card slots. Levy teaches switch (116) connected to interconnect and adapted to convert interconnect lanes into plurality of distributed links such that there is a different one of distributed links providing connection to each of plurality of high-speed video card slots [0021, 0017, 0018, 0016]. Fig. 2 of Levy shows that devices transmit data to other devices by connecting their ports through links [0018]. Fig. 3 shows that ports transmit data through port transmitters 116 and ports receive data through port receivers [0021]. Therefore, devices transmit data to other devices by connecting their port transmitters 116 to port receivers on other devices through links [0018, 0021]. Port identification is performed by a port receiving a child ID and updating the device mapping table to indicate which port on the device is connected to which port on which device as indicated by the child ID response received from the device that the device is to be connected to, and then connecting the ports as indicated by the mapping table in order to transmit data to the indicated device [0041, 0044, 0074, 0075]. Since devices transmit data to other devices by connecting their port transmitters 116 to port receivers on other devices [0018, 0021], this means that port transmitters 116 perform the port

identification. In order to indicate which port of the device is connected to which port on which device for port identification [0041, 0044, 0074, 0075], the ports need to determine where the port transmitters 116 are connected (Figs. 2-3) [0018, 0021]. Thus, ultimately, the port transmitters 116 are performing the port identification. The entirety of [0075] of Levy recites: "At this point, port identification is complete and lanes of the links between the DEVICES 0-5 are defined. In particular, LINK 1 consists of three lanes, LINK 2 consists of two lane, LINK 3 consists of two lanes, LINK 4 consists of one lane, and LINK 5 consists of one lane. The above embodiments enable a system designer to route signal lines between ports with minimal limitations imposed by the location of the device ports. In general, the system designer may simply interconnect ports in a manner that eases physical routing and allow the port identification methods of the devices discover/identify the portion connections. Further, the port identification methods provide the system designer with fine grain control of bandwidth between devices by allowing the system designer to assign lanes to links of a per lane basis." Therefore, interconnect lanes are converted into a plurality of distributed links such that there is a different one of said distributed links providing a connection to each of said plurality of high-speed video cards slots through the port identification method [0021, 0017, 0018, 0016, 0075]. Since the port transmitters 116 perform the port identification, this meant that the port transmitter 116 is capable of converting the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection each of said plurality of high-speed video cards slots. Levy teaches performing port identification to define lanes of links between devices, and assigns certain number of lanes to each link. Port identification methods provide system designer with fine grain control of bandwidth between devices by allowing

system designer to assign lanes to links on per lane basis [0075]. One or more devices (DEVICES 1-5) comprise video cards [0016]. Devices may initiate their port identification methods in response to events other than in response to power on reset, such as, for example, root reset or request to re-identify its ports. Device ID of the device may be set by reset hardware of the device, or may be set by some other mechanisms [0042]. So, lanes are distributed not only during startup or other one-time configuration of machine, but during operation (devices may initiate their port identification methods in response to other events such as, for example, root reset or request to re-identify its ports [0042]). So, Levy teaches switch is configured to distribute lanes dynamically during operation to plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by video cards [0075, 0016, 0042]. Levy teaches that devices may initiate their port identification methods in response to events other than in response to power on reset, such as, for example, root reset or request to re-identify its ports [0042]. Therefore, devices do not have to turn off and then turn on in order to initiate their port identification methods. Therefore, devices can be powered on the entire time while they initiate their port identification methods. Since the devices are powered on the entire time, this is taken to mean that the devices are operating or processing the entire time. The Examiner respectfully points out that since there does not seem to be support for distributing lanes dynamically <u>during data transmission</u> in the instant specification, as discussed above, this limitation will not be addressed for the 35 U.S.C. 103(a) rejections. Levy teaches that a switch (116) is configured to distribute lanes, as discussed above. Levy teaches that the switch is configured to distribute different numbers of lanes to different ports of different devices, and can change this distribution [0075, 0042], and therefore the switch is configured to distribute lanes

dynamically. Levy describes "port identification methods provide the system designer with fine grain control of bandwidth between devices" [0075], and therefore the lanes are distributed responsive to changes in bandwidth needs. Therefore, Levy teaches that the request to re-identify its ports is performed by a switch configured to distribute lanes dynamically during operation to said plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by said video cards [0075, 0016, 0042].

However, Levy does not teach computing device is motherboard and motherboard enables first and second card to attach, respectively, to at least one first card slot and second card slot, and motherboard enables first and second card to operate concurrently to output data. However, Stufflebeam teaches interconnect connecting to motherboard (*host bus 110 typically is located on a motherboard*, col. 4, lines 48-50; *memory controller 200 provides interconnection between the host bus 110*, col. 4, lines 59-61); and plurality of high-speed card slots connected to interconnect (col. 6, lines 23-35). When user wishes to attach additional card, power is removed from card slot that card is to be attached to. After inserting card into slot, the software identifies and configures the additional card in the slot so that the first and second card can operate in parallel to output data (*power-down applet receives signal from a user indicating a user desire to insert an additional card into a PCI slot*, col. 3, lines 31-33, col. 3, line 56-col. 4, line 17; *processing parallelism*, col. 1, lines 21-25), and the cards can include video cards (col. 5, lines 7-19).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Levy so computing device is motherboard as suggested by Stufflebeam. Motherboards are well-known in the art and widely used. Motherboards make it easy to add new

features to machine over time. Motherboards have opened the computer to creative opportunities for third-party vendors. Motherboard, by enabling pluggable components, allows users to personalize a computer system depending on their applications and needs. It would have been obvious to modify Levy so motherboard enables 1st and 2nd card to attach, respectively, to at least one first card slot and second card slot, and motherboard enables first and second card to operate concurrently to output data because Stufflebeam suggests faster processing (col. 1, lines 21-25).

However, Levy and Stufflebeam do not expressly teach both cards are video cards, and video cards output graphics data to a single visual display device. However, Grimaud teaches attaching a first and a second video card to at least one first video card slot and second video card slot, respectively, wherein the first and second video cards operate in parallel to output graphics data to a single visual display device (col. 2, lines 40-44, col. 2, lines 53-65; col. 7, lines 39-40).

It would have been obvious to modify devices of Levy and Stufflebeam so display area of display is divided into first and second sections, first video card performing graphics processing related to first section; and second video card performing graphics processing related to second section because Grimaud suggests this ensures single graphics element is not overburdened with its rendering task by allowing dynamic adjustment of each graphics element so graphics elements take approximately the same time to render their respective images, and video cards can operate on these divided sections in parallel, therefore allowing different graphics machines to be connected together to render complex images faster than any one of them taken separately would be able to render (col. 5, line 55-col. 6, line 12; col. 7, lines 10-40).

12. As per Claims 3, 53, and 55, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect comprising a x16 connection and said first and second high-speed video card slots are each physically configured as x16 video card slots, and wherein the switch (116, Fig. 3) dynamically distributes bandwidth from the x16 connection to two x16 video card slots via said distributed links [0001, 0021, 0017, 0018, 0016, 0075, 0042]. Levy describes devices may initiate their port identification methods in response to events other than in response to power on reset, such as, for example, a root reset or a request to re-identify its ports. The device ID of the device may be set by reset hardware of the device, or may be set by some other mechanisms [0042]. So, lanes are distributed not only during startup or other one-time configuration of machine, but can be redistributed several times during operation, whenever there is a root reset or a request to re-identify its ports [0042]. So, the lanes are dynamically distributed. So, Levy teaches a switch that dynamically distributes the bandwidth [0075, 0042].

13. As per Claim 4, Levy teaches interconnect comprises at least a x32 connection [0001].

14. As per Claim 5, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect that is divided into two or more x16 connections between the chipset (104, Fig. 1) and the plurality of high-speed video card slots [0001, 0014, 0016].

15. As per Claim 6, Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links,

leaving chips to optionally support other link widths. So, Levy teaches interconnect comprising at least a x16 connection, and wherein the interconnect is divided into a x8 connection between the chipset and each of the plurality of high-speed video card slots [0001, 0016].

16. As per Claims 7, 54, and 56, Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches interconnect having a connection having at least 24 lanes, and wherein said switch dynamically distributes lanes at any given time during operation [0075, 0042] into x8 connection between chipset (104, Fig. 1) and one of plurality of high-speed video card slots and x16 connection between chipset and another of plurality of high-speed video card slots [0001, 0016].

17. As per Claim 29, Levy teaches interconnect supports links between chips that have x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches wherein the switch allocates 1st x16 connection to 1st video card slot and 2nd smaller-scaled connection to 2nd video card slot [0075, 0001, 0016].

18. As per Claims 30 and 46, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Levy gives an example wherein the second connection is a x4 connection. Therefore, Levy discloses a second connection that is at least one of a x1, x2, x4, and x8 connection [0001].

19. As per Claims 32 and 47, Levy teaches that the interconnect (Device 0) connects to Devices 1-5. Devices 1-5 could be Ethernet cards, video cards, RAID controllers, SCSI

controllers, ATA disk controllers, PCI bridges, etc. [0016]. Therefore, it would be obvious to one of ordinary skill in the art that Device 1 and Device 2 could each be a video card, and Device 3 could be a peripheral. Levy describes that the device interfaces of the Devices 0-5 support lane reordering. For example, the device interface of Device 0 may support up to 4 links, and Device 1 may support up to 3 links [0020]. For example, Link 1 consists of three lanes, Link 2 consists of two lanes, Link 3 consists of two lanes, Link 4 consists of one lane, and Link 5 consists of one lane [0075]. Since the device interfaces of the Devices 0-5 support lane reordering [0020], it would be obvious to one of ordinary skill in the art that the dimensions of the lanes can be specified to be any dimension that is needed to support cards and peripherals of various dimensions. Therefore, Device 1 and Device 2 could have first prespecified dimensions, and Device 3 could have second prespecified dimensions. Therefore, it would be obvious to one of ordinary skill in the art from the device of Levy to further comprise a peripheral slot connected to the interconnect (Device 0), wherein the first video card slot and the second video card slot have first prespecified dimensions and the peripheral slot has second prespecified dimensions, wherein the second dimensions differs from the first dimensions [0016, 0020, 0075].

However, Levy does not expressly teach that two cards are video cards. However, Grimaud teaches attaching a first and a second video card to at least one first video card slot and second video card slot, respectively (col. 2, lines 40-44, col. 2, lines 53-65; col. 7, lines 39-40). This would be obvious for the reasons given in the rejection for Claim 1.

20. As per Claim 33, Levy teaches that a graphics card can be coupled to any of the video card slots [0016, 0020]. Therefore, Levy teaches wherein the first video card slot and the second video card slot have first prespecified dimensions [0016, 0020, 0075], as discussed in the

rejection for Claim 32, and wherein the first dimensions of the video card slots that are selected to allow a graphics card to be coupled to any of the video card slots [0016, 0020].

21. As per Claim 34, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses a graphics card that is designed to be used with a x16 connection [0001, 0016].

22. A per Claim 41, Levy teaches computing device for supporting multiple video cards, computing device having processor socket 104 adapted to receive processor 102 [0014]; single scalable interconnect (Device 0) provides data paths to processor socket (Fig. 1), said scalable interconnect supporting a number of interconnect lanes [0021, 0018]; plurality of high-speed video card slots connected to interconnect, each video card slot has first prespecified dimensions and is specifically adapted for coupling to video card [0001, 0021, 0016]. Levy teaches a switch (116) connected to said interconnect and adapted to convert the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection to each of said plurality of high-speed video card slots [0021, 0017, 0018, 0016], as discussed in the rejection for Claim 1, and wherein said switch is configured to distribute lanes dynamically during operation to said plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by said video cards [0075, 0016, 0042]. The Examiner respectfully points out that since there does not seem to be support for distributing lanes dynamically <u>during data transmission</u> in the instant specification, as discussed above, this limitation will not be addressed for the 35 U.S.C. 103(a) rejections.

However, Levy does not teach that the computing device is a motherboard, the processor is a central processing unit (CPU), and the motherboard is capable of receiving and facilitating concurrent operation of a first and a second card to output data. However, Stufflebeam describes that the computing device is a motherboard (col. 4, lines 48-50), the processor is a central processing unit (CPU) (100, Fig. 1; col. 4, lines 40-46), and the motherboard is capable of receiving and facilitating concurrent operation of a first and a second card to output data (col. 3, lines 31-33, col. 3, line 56-col. 4, line 17; col. 1, lines 21-25), wherein the cards can include video cards (col. 5, lines 7-19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Levy so the processor is a CPU as suggested by Stufflebeam. CPUs are well-known in the art and are widely used. The CPU is the brains of the computer. The CPU is needed to perform most of the calculations. In terms of computing power, the CPU is the most important element of a computer system. It would have been obvious to modify the device so that the motherboard is capable of receiving and facilitating concurrent operation of a first and a second card to output data for the same reasons given in the rejection for Claim 1.

However, Levy and Stufflebeam do not teach that the cards are substantially similar video cards and operate to output graphics data to a single visual display device. However, Grimaud teaches this limitation, as discussed in the rejection for Claim 1.

23. As per Claim 44, Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths, so, Levy teaches each of video card slots is configured to couple with graphics card designed to be used with x16 connection [0001, 0016].

24. As per Claim 45, Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches an interconnect (Device 0, Fig. 1) and said switch produce a first data path (Link 1) and a second data path (Link 2), each of the first and second data paths connecting the processor socket (104) to different video card slots, the first data path being equal to or larger in scale than the second path [0001, 0016].

25. As per Claim 48, Levy teaches high performance computer including scalable interconnect (Device 0) that supports number of interconnect lanes [0021, 0018], scalable interconnect connects to first and second high-speed video card slots via switch, first and second high-speed video card slots having substantially similar physical configuration [0001], as discussed for Claim 42, and video slot physical configuration is selected to allow first and second high-speed video card slots each to accept a graphics card; and first graphics card coupled to first high-speed video card slot [0016]; the following occurs during operation of said computer: said switch converts said interconnect lanes into two distributed links such that there is a different one of said distributed links connecting to each of said plurality of high-speed video card slots [0021, 0017, 0018, 0016], as discussed in the rejection for Claim 1, and switch distributes lanes to said distributed links in response to current bandwidth needs of said graphics cards during processing by said cards [0075, 0016, 0042].

However, Levy does not teach computing device is motherboard, processor is central processing unit (CPU), and second graphics card coupled to second high-speed video card slot, wherein the following occurs during operation of said computer: said first and second graphics cards operate concurrently to output graphics data to a display device. However, Stufflebeam

teaches that the computing device is a motherboard (col. 4, lines 48-50), the processor is a CPU (100, Fig. 1; col. 4, lines 40-46), and a second card coupled to the second slot, wherein the following occurs during operation so said computer: said first and second cards operate concurrently to output data (col. 3, lines 31-33, col. 3, line 56-col. 4, line 17; col. 1, lines 21-25), wherein the cards can include high-speed graphics cards (col. 5, lines 7-19). This would be obvious for reasons for Claim 41.

26. As per Claims 50-52, Levy does not teach a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the first section; and the second video card performing graphics processing related to the second section. However, Grimaud teaches a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the first section; and the second video card performing graphics processing related to the second section (col. 2, lines 40-44, 53-65). This would be obvious for same reasons given in the rejection for Claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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JH

/Joni Hsu/
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